LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. An identifier indicating the status of each claim is provided.

Listing of Claims

1. (Currently Amended) A distortion compensation circuit for generating a predistortion signal to perform distortion compensation of a power amplifier comprising:

A/D converter means for digitizing a voltage value of a signal after quadrature modulating a baseband signal;

subtractor means supplied with the output data of the A/D converter means;

voltage value data output means for outputting a voltage value data corresponding to the output data of the subtractor means by selecting from a plurality of pieces of previously stored voltage value data;

amplitude impulse response accumulation adding means for outputting an accumulation adding value of multiplication values obtained by multiplying the signal voltage value after quadrature modulation by impulse response values corresponding to amplitude characteristic of the power amplifier in accordance with the voltage value data from the signal voltage value data outputting means and supplying to the subtractor means; and

D/A converter means for converting the voltage value data from the voltage value data outputting means into an analog signal as an output predistortion signal regarding the amplitude component of the power amplifier.

wherein said amplitude impulse response accumulation adding means comprises:

N of first table blocks each having a first table storing M of said multiplication values corresponding to each of said voltage value data and a first adder for adding M of said multiplication values outputted from said first table;

a delay block formed by serially connecting N-1 of delays for delaying the voltage value data outputted from said voltage value data output means by a predetermined time; and

a second adder for outputting said accumulation adding values obtained by adding respective output values from respective first adder in said N of first table blocks to said subtractor means, and N of points comprising input point of said delay at a first stage, each of connecting points among delays, and output point of said delay at final stage in the delay block are connected to each of input point in said N of first table block, and at least a part of the voltage value data outputted from said voltage value data output means is defined as address data for accessing each of said first table in said first table block, wherein said M and N are natural numbers.

2. (Original) The distortion compensation circuit as cited in claim 1, further comprising:

phase impulse response accumulation adding means for outputting accumulation adding values of converted values obtained by changing code of the impulse response values depending on the voltage value after quadrature modulation and a phase characteristic of said

power amplifier in response to the voltage value data from said voltage value data output means; and

phase shift means for phase-shifting a phase of the predistortion signal regarding the amplitude component supplied to the power amplifier based on the accumulation adding values from said phase impulse response accumulation adding means.

3. (Canceled)

4. (Original) ~~The distortion compensation circuit as cited in claim 2,~~ A distortion compensation circuit for generating a predistortion signal to perform distortion compensation of a power amplifier comprising:

A/D converter means for digitizing a voltage value of a signal after quadrature modulating a baseband signal;

subtractor means supplied with the output data of the A/D converter means;

voltage value data output means for outputting a voltage value data corresponding to the output data of the subtractor means by selecting from a plurality of pieces of previously stored voltage value data;

amplitude impulse response accumulation adding means for outputting an accumulation adding value of multiplication values obtained by multiplying the signal voltage value after quadrature modulation by impulse response values corresponding to amplitude

characteristic of the power amplifier in accordance with the voltage value data from the signal voltage value data outputting means and supplying to the subtractor means;

D/A converter means for converting the voltage value data from the voltage value data outputting means into an analog signal as an output predistortion signal regarding the amplitude component of the power amplifier;

phase impulse response accumulation adding means for outputting accumulation adding values of converted values obtained by changing code of the impulse response values depending on the voltage value after quadrature modulation and a phase characteristic of said power amplifier in response to the voltage value data from said voltage value data output means; and

phase shift means for phase-shifting a phase of the predistortion signal regarding the amplitude component supplied to the power amplifier based on the accumulation adding values from said phase impulse response accumulation adding means,

whererin ~~wherein:~~ said amplitude impulse response accumulation adding means comprises:

N of first table blocks each having a first table storing M of said multiplication values corresponding to each of said voltage value data and a first adder for adding M of said multiplication values outputted from said first table;

a delay block formed by serially connecting N-1 of delays for delaying the voltage value data outputted from said voltage value data output means by a predetermined time; and

a second adder for outputting said accumulation adding values obtained by adding respective output values from respective first adder in said N of first table blocks to said subtractor means, and N of points comprising input point of said delay at a first stage, each of connecting points among delays, and output point of said delay at final stage in the delay block are connected to each of input point in said N of first table block, and at least a part of the voltage value data outputted from said voltage value data output means is defined as address data for accessing each of said first table in said first table block, wherein said M and N are natural numbers.

5. (Currently Amended) The distortion compensation circuit as cited in ~~claim 3~~ claim 1,

wherein ~~, wherein:~~ said amplitude impulse response accumulation adding means comprises: N of second table blocks each having a second table storing M of said multiplication values corresponding to each of said voltage value data and a second adder for adding M of said multiplication values outputted from said second table; a second adder for outputting said accumulation adding values obtained by adding respective output values from respective second adder in said N of second table blocks to said subtractor means, and N of points comprising input point of said delay at a first stage, each of connecting points among delays, and output point of said delay at final stage in the delay block are connected to each of input point in said N of second table block, wherein said M and N are natural numbers.

6. The distortion compensation circuit as cited in ~~claim 3, wherein:~~ claim 1,

wherein said amplitude impulse response accumulation adding means comprises: N of second table blocks each having a second table storing M of said multiplication values corresponding to each of said voltage value data and a second adder for adding M of said multiplication values outputted from said second table; a second adder for outputting said accumulation adding values obtained by adding respective output values from respective second adder in said N of second table blocks to said subtractor means, and N of points comprising input point of said delay at a first stage, each of connecting points among delays, and output point of said delay at final stage in the delay block are connected to each of input point in said N of second table block, wherein said M and N are natural numbers.

7. (Currently Amended) A transmission apparatus for transmitting a signal which is amplified by a power amplifier comprising:

a quadrature modulation section for quadrature-modulating a baseband signal;

a distortion compensation section including:

A/D converter means for digitizing a voltage value of a signal from said quadrature modulation section;

subtractor means supplied with the output data of the A/D converter means;

voltage value data output means for outputting a voltage value data corresponding to the output data of the subtractor means by selecting from a plurality of pieces of previously stored voltage value data;

amplitude impulse response accumulation adding means for outputting an accumulation adding value of multiplication values obtained by multiplying the signal voltage

value after quadrature modulation by impulse response values corresponding to amplitude characteristic of the power amplifier in accordance with the voltage value data from the signal voltage value data outputting means and supplying to the subtractor means; and

D/A converter means for converting the voltage value data from the voltage value data outputting means into an analog signal as an output predistortion signal regarding the amplitude component of the power amplifier; and a conversion/removing section supplied with the output signal from the distortion compensation section for effecting frequency conversion and removal of electromagnetic interference and for transmitting to the power amplifier,

wherein said amplitude impulse response accumulation adding means comprises:

N of first table blocks each having a first table storing M of said multiplication values corresponding to each of said voltage value data and a first adder for adding M of said multiplication values outputted from said first table;

a delay block formed by serially connecting N-1 of delays for delaying the voltage value data outputted from said voltage value data output means by a predetermined time; and

a second adder for outputting said accumulation adding values obtained by adding respective output values from respective first adder in said N of first table blocks to said subtractor means, and N of points comprising input point of said delay at a first stage, each of connecting points among delays, and output point of said delay at final stage in the delay block are connected to each of input point in said N of first table block, and at least a part of the voltage value data outputted from said voltage value data output means is defined as address data

for accessing each of said first table in said first table block, wherein said M and N are natural numbers.